MP1181
A190 Packet Tunnel Engine

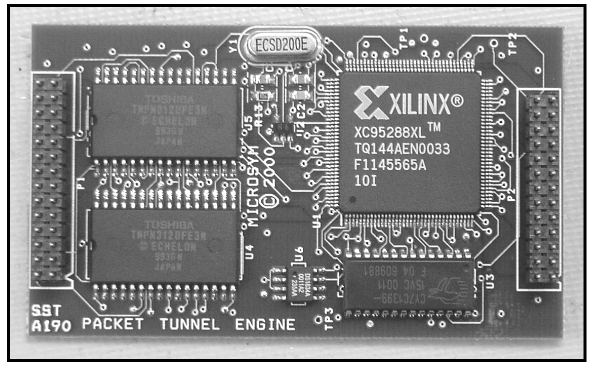
Data Sheet and User's Guide
2002-02-11, Version 2

Features

- Facilitates implementation of tunneling EIA-709 routers over foreign protocols
- Maximum throughput of 12-byte packets via Echelon® RTR-10 Router Core Modules:
  - 640 packets per second (unidirectional)
  - 800 packets per second (bidirectional)
- Includes 64-packet FIFO buffer
- Full duplex synchronous NRZ data link to the foreign protocol interface.
- Will accept data from the foreign protocol interface at rates from 0 to 8.196Mbps
- Smaller than a credit card, with a mounted vertical profile of 3/8" (9.5mm)
- Solders to target PCB via two dual-row headers
- Low power consumption, requiring 5VDC and 3.3VDC
- Fully compatible with Echelon LNS™ based network management tools
- -40°C to +85°C ambient operating temperature range
- No sockets for mechanical reliability
- All capacitors are ceramic
- Can be conformally coated
- Lamp test function
- Health status output
- Three FIFO buffer status outputs (not empty, half full, full)
- Neuron Chip® EEPROM refresh function provided to enhance long-term reliability
- On-board CPLD, with 20 year program data retention
- On-board low-voltage detector and reset generator
- No Echelon licenses required
- Direct interface to Echelon RTR-10
- LED driver circuit provided in support of Echelon RTR-10 PKT signal

Description

The A190 is a packet tunnel engine, intended to facilitate the implementation of tunneling EIA-709 (LonTalk®) routers over foreign protocols. Designed to be used in conjunction with the Echelon RTR-10 Router Core Module, the A190 communicates to the foreign protocol interface via a full-duplex NRZ serial data link.



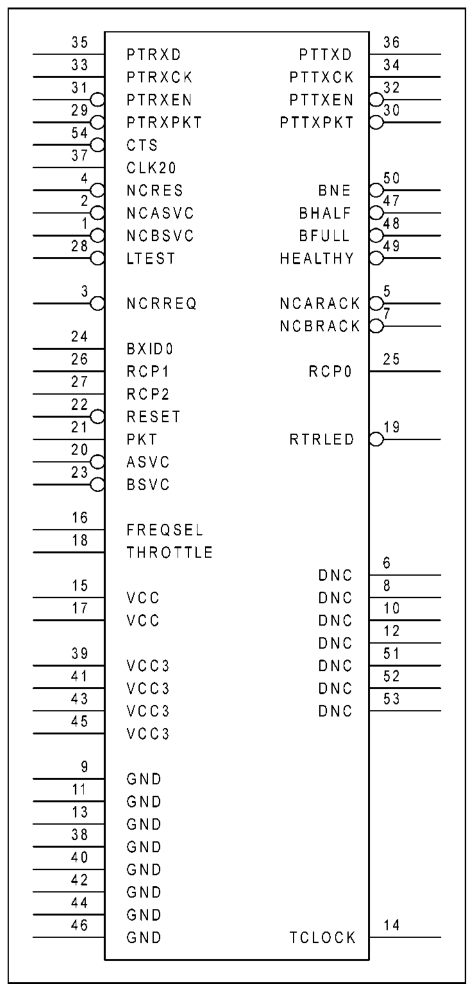


Figure 1: A190 Schematic Symbol

Reliability

The A190 is designed with rugged applications in mind. It can be soldered to the target PCB, it uses no sockets, and it can be conformally coated.

All capacitors are ceramic, providing long-term reliability and stability over temperature.

The A190 supports refresh of its Neuron Chip EEPROM, using three interface signals. This can be done as a maintenance function every few years. If this is not done, then the Neuron Chip EEPROM may begin to lose data after 10 years.

A CPLD is used to implement certain logic functions on the A190. The program data retention rating of this CPLD is 20 years.

The construction of the A190, along with the industrial ambient operating temperature range, makes it suitable for use in many industrial and transportation applications.

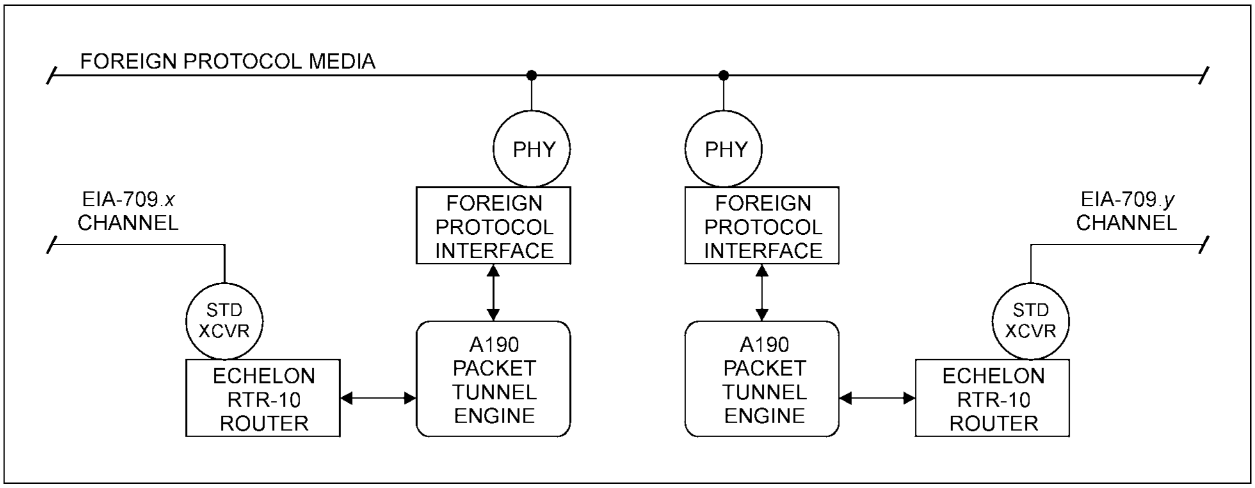


Figure 2: System Application

System Application Overview

The A190 fits into the system between an Echelon router and a foreign protocol interface as shown in figure 2.

The connection to the foreign protocol interface consists of four transmit signals and four receive signals. These signals provide a full-duplex synchronous NRZ serial interface. Two A190s can be connected directly together back-to-back, simply by crossing over these signals between them. Therefore, the foreign protocol interface can be as simple or as complex as needed, depending on the requirements of the foreign protocol.

From the point of view of an Echelon LNS based network management tool, all of the A190s appear as a single TP/RS485-1250 channel. The only difference is that the channel delay must be set to account for the propagation delay through the A190s and the foreign protocol. In other words, the RTR-10s appear to be connected together on one TP/RS485-1250 channel, which has some additional channel delay.

Signal Descriptions

All A190 interface signals are TTL compatible. Table 1 provides a summary of the signals.

Note that the A190 contains two Neuron Chip devices. These are referred to as 'Neuron Chip A' and 'Neuron Chip B'. These should not be confused with the A and B sides of the RTR-10.

Table 1: Signal List

Pin Name	#	I/O	Description
NCBSVC	1	I/O	Active low SERVICE signal on Neuron Chip B. NCBSVC is connected to a 4.7KΩ pullup resistor to VCC.
NCASVC	2	I/O	Active low SERVICE signal on Neuron Chip A. NCASVC is connected to a 4.7KΩ pullup resistor to VCC.
NCRREQ	3	IN	Active low EEPROM refresh request. NCRREQ is connected to a 4.7KΩ pullup resistor to VCC.
NCRES	4	I/O	Active low RESET signal connected to both Neuron Chip A and Neuron Chip B. NCRES is connected to a 4.7KΩ pullup resistor to VCC, and a reset generator.
NCARACK	5	Out	Active low EEPROM refresh acknowledge from Neuron Chip A.
DNC	6	I/O	Do Not Connect (for manufacturing test purposes)
NCBRACK	7	Out	Active low EEPROM refresh acknowledge from Neuron Chip B.
DNC	8	I/O	Do Not Connect (for manufacturing test purposes)
GND	9	In	Ground reference and VCC, VCC3 power return
DNC	10	I/O	Do Not Connect (for manufacturing test purposes)
GND	11	In	Ground reference and VCC, VCC3 power return
DNC	12	I/O	Do Not Connect (for manufacturing test purposes)
GND	13	In	Ground reference and VCC, VCC3 power return
TCLOCK	14	Out	Throttle clock output. Either 10KHz or 100Hz, as selected using the FREQSEL input.
VCC	15	In	5VDC power
FREQSEL	16	In	Tie high or leave open to configure TCLOCK as a 10KHz output. Tie to ground to configure TCLOCK as a 100Hz output. FREQSEL is connected to a 4.7KΩ pullup resistor to VCC.
VCC	17	In	5VDC power
THROTTLE	18	In	Throttle clock input. This clock controls the maximum rate at which the A190 will deliver packets to the RTR-10.
RTRLED	19	Out	Active low, open-collector output intended to drive a router activity LED. This output pulses low for at least 9.8ms while transitions are being detected on the PKT input.
ASVC	20	In	Active low input, which should be connected to the ASVC signal on the RTR-10. ASVC is connected to a 4.7KΩ pullup resistor to VCC.
PKT	21	I/O	Transition detect input, which should be connected to the PKT signal on the RTR-10. PKT is driven to the same level as BXID0 for 50ns, immediately following the rising edge of RESET. This prevents the CPLD bus-hold input circuit connected to PKT from interfering with the RTR-10 transceiver configuration process.
RESET	22	In	Active low input, which should be connected to the RESET signal on the RTR-10. Note that a low voltage detector must still be provided for the RTR-10.
BSVC	23	In	Active low input, which should be connected to the BSVC signal on the RTR-10. BSVC is connected to a 4.7KΩ pullup resistor to VCC.
BXID0	24	In	RTR-10 B-side transceiver ID bit 0 input. This should be connected to BXID0 on the RTR-10.
RCP0	25	Out	Receive data output, which should be connected to the ACP0/BCP0 signal on the RTR-10. This signal is source terminated, so it should not be connected to any other loads.
RCP1	26	In	Transmit data input, which should be connected to the ACP1/BCP1 signal on the RTR-10.
RCP2	27	In	Active high transmit enable input, which should be connected to the ACP2/BCP2 signal on the RTR-10.
LTEST	28	In	Active low lamp test input. Pulling LTEST low will cause the NCASVC, NCBSVC, RTRLED, HEALTHY, BFULL, BHALF, and BEMPTY signals to go low. LTEST is connected to a 4.7KΩ pullup resistor to VCC.
PTRXPKT	29	In	Active low input, which is used to frame packets being sent to the A190 from the foreign protocol interface.
PTTXPKT	30	Out	Active low output, which is used to frame packets being sent from the A190 to the foreign protocol interface. This signal is source terminated, so it should be connected to only one load.

Pin Name	#	I/O	Description
PTRXEN	31	In	Active low input, which is driven by the foreign protocol interface to indicate that it is operational and ready to communicate.
PTTXEN	32	Out	Active low output, which is used to tell the foreign protocol interface that the A190 is operational and ready to communicate. PTTXEN will be low if neither the Neuron Chips nor the RTR-10 are in reset. This signal is source terminated, so it should be connected to only one load.
PTRXCK	33	In	Rising edge clock input. This is used by the foreign protocol interface to indicate when PTRXD and PTRXPKT should be sampled by the A190.
PTTXCK	34	Out	Rising edge clock output. Upon detection of rising PTTXCK edges, the foreign protocol interface must sample both PTTXD and PTTXPKT. PTTXCK is source terminated, so it should be connected to only one load.
PTRXD	35	In	Data input, which receives NRZ data from the foreign protocol interface.
PTTXD	36	Out	Data output, which transmits NRZ data to the foreign protocol interface. This signal is source terminated, so it should be connected to only one load.
CLK20	37	In	20MHz clock input. This input must be driven by a 20.000MHz ±100ppm clock source. The duty cycle must be in the range of 35% to 65%.
GND	38	In	Ground reference and VCC, VCC3 power return
VCC3	39	In	3.3VDC power
GND	40	In	Ground reference and VCC, VCC3 power return
VCC3	41	In	3.3VDC power
GND	42	In	Ground reference and VCC, VCC3 power return
VCC3	43	In	3.3VDC power
GND	44	In	Ground reference and VCC, VCC3 power return
VCC3	45	In	3.3VDC power
GND	46	In	Ground reference and VCC, VCC3 power return
BHALF	47	Out	Active low open-collector buffer half-full output that indicates that there are 32 to 63 packets queued in the A190 FIFO. This can be used to drive a status LED.
BFULL	48	Out	Active low open-collector buffer full output that indicates that there are 64 packets queued in the A190 FIFO. This can be used to drive a status LED.
HEALTHY	49	Out	Active low open-collector output that indicates that the A190 is probably healthy and operational. This can be used to drive a status LED.
BNE	50	Out	Active low open-collector buffer not-empty output that indicates that there is at least one packet queued in the FIFO. This output pulses low for at least 9.8ms, and can be used to drive an activity LED.
DNC	51	I/O	Do Not Connect (for manufacturing test purposes)
DNC	52	I/O	Do Not Connect (for manufacturing test purposes)
DNC	53	I/O	Do Not Connect (for manufacturing test purposes)
CTS	54	In	Active low Clear-To-Send input that is used to enable data flow from PTTXD. While CTS is high, the A190 will not begin to transmit a new packet to the foreign protocol interface. Taking CTS high during a packet transmission will not interrupt that packet, but will prevent a new packet transmission until CTS is taken low.

DETAILED DESCRIPTION

Packet Transmission

Transmission is considered to be movement of packets from the RTR-10 to the foreign protocol interface.

All packets transmitted by the RTR-10 (ACP1/BCP1) are converted to NRZ data in real time, and sent to the foreign protocol interface. The foreign protocol interface can use the CTS signal to delay packet transmission. Note that packets can be lost if CTS is held high for long periods of time.

The nominal PTTXCK rate is 1.25MHz. This is a nominal period of 800ns, but this can occasionally shift ±50ns, as a result of the synchronization of BCP1 data to the A190 20MHz clock.

At the start of a packet, the A190 will pull PTTXPKT low, and present the first bit on PTTXD. The A190 will then pulse PTTXCK low. For all remaining bits the A190 will keep PTTXPKT low, present data on PTTXD, and pulse PTTXCK low. After the last bit, the A190 will set PTTXPKT high, and pulse PTTXCK low one last time.

Packet Reception

Reception is considered to be movement of packets from the foreign protocol interface to the RTR-10.

The A190 buffers all packets received from the foreign protocol interface in FIFO RAM. A packet is not queued for delivery to the RTR-10 until the entire packet is loaded into the FIFO. As a result, the bit rate at which the foreign protocol interface delivers the data can be from 0 to 8.196MHz, and can be delivered in bursts.

At the start of a packet, the foreign protocol interface must pull PTRXPKT low, and present the first bit on PTRXD. The foreign protocol interface must then pulse PTRXCK low. For all remaining bits the foreign protocol interface must keep PTRXPKT low, present data on PRTXD, and pulse PTRXCK low. After the last bit has been clocked, the foreign protocol interface must set PTRXPKT high, and pulse PTRXCK low one last time.

The A190 has enough RAM to buffer 64 packets. The maximum size of each packet, including preamble bits and data, is 4064 bits.

There are three status outputs (open-collector) that indicate how many packets are queued in the FIFO. BNE is low when at least one packet is in the FIFO. BHALF is low when there are between 32 and 63 packets in the FIFO. BFULL is low if all 64 packets are in the FIFO. If all buffers are in use then the A190 will discard any further packets received from the foreign protocol interface.

When a packet buffer is ready the A190 converts the data to differential Manchester format and delivers the data to the RTR-10 (ACP0/BCP0). If a collision is detected during this time then the buffer is not freed and the packet is sent to the RTR-10 again. If no collision is detected then the buffer is freed.

Throttle

The A190 has no way of knowing if the RTR-10 has a buffer available to store each message sent to the RTR-10. Therefore, there will be packets lost by the RTR-10 in applications where the A190 is delivering messages to the RTR-10 faster than the RTR-10 can deliver them to the EIA-709.*x* channel. This can be a significant problem for channels with bit rates less than 1.25Mbps. To compensate for this, the A190 has a THROTTLE input, which can be used to control the maximum rate at which messages are delivered to the RTR-10.

The THROTTLE input should be a clock with a nominal duty cycle of 50%. If fewer than 8 packets are queued in the FIFO, then the maximum rate at which the A190 will deliver packets to the RTR-10 will be equal to the THROTTLE clock frequency. If 8 or more packets are queued in the FIFO, then the maximum rate at which the A190 will deliver packets to the RTR-10 will be equal to twice the THROTTLE clock frequency.

The A190 has a clock output (TCLOCK) which can be used to drive the THROTTLE input. Immediately following reset, the A190 examines the FREQSEL input to configure the TCLOCK output. If FREQSEL is high or left unconnected, then TCLOCK is set to 10KHz. Use this for an RTR-10 connected to a 1.25Mbps channel. If FREQSEL is low, then TCLOCK is set to 100Hz. This is recommended when the RTR-10 is connected to a 78Kbps channel. The THROTTLE input can be driven by a different clock frequency if desired, but the minimum THROTTLE clock frequency is 6Hz. For applications where messages should be forwarded as fast as possible, use the 10KHz clock.

In applications where the RTR-10 is used as a bridge or a configured router, the rate at which packets are delivered to the EIA-709.*x* channel by the RTR-10 will be lower than the THROTTLE controlled rate. How much lower will be dictated by the number of messages delivered by the A190 to the RTR-10, versus the number of these messages that the RTR-10 forwards through to the EIA-709.*x* channel. In these cases it may be desirable to increase the THROTTLE frequency accordingly.

Health Monitor Logic

There is a HEALTHY output (open-collector) that is driven by health monitor logic in the A190. This logic monitors some basic operational characteristics, and pulls HEALTHY low if these are all okay. HEALTHY will be low if all of the following are true:

- The A190 CPLD is programmed and configured
- The NCRES signal is high
- The RESET signal is high
- The NCASVC signal is high
- The NCBSVC signal is high
- The ASVC signal is high
- The BSVC signal is high
- The A190 Neuron Chips are providing heartbeat signals to the A190 CPLD

EEPROM Refresh

The EEPROM in the A190 Neuron Chip devices may begin to lose data after 10 years. The A190 provides a refresh function for the EEPROM memory, which can be used to extend the useful life of the A190.

Immediately following reset, the A190 Neuron Chips examine the state of signal NCRREQ. If NCRREQ is low, then they will execute the EEPROM refresh function. While the EEPROM refresh is in progress, Neuron Chip A will pull NCARACK low, and Neuron Chip B will pull NCBRACK low. Once NCARACK and NCBRACK are low, NCRREQ does not need to be kept low.

During the refresh period the A190 will not transport packets from the foreign protocol interface to the RTR-10, and the HEALTHY signal will not be pulled low. The time required for the refresh function will vary significantly depending on several factors. Following the refresh operation, the A190 will begin normal operation.

The maximum number of times that the EEPROM may be refreshed is limited to 10,000. Therefore, the refresh operation should be used sparingly.

Power

Both 5VDC and 3.3VDC are required by the A190. VCC3 startup should be monotonic, to ensure proper CPLD configuration. If a dedicated low-dropout regulator is being used to supply VCC3, then a regulator with an output current rating of 500mA (minimum) is recommended. A 300mA regulator may be insufficient to handle peak current requirements over all operating conditions.

The total decoupling capacitance between VCC3 and GND is 3μF ±10%. The total decoupling capacitance between VCC and GND is 2.2μF ±10%. All capacitors are X7R ceramic dielectric.

Neuron Chip Details

The Neuron Chip devices on the A190 do not require network installation or management. This is handled automatically by the A190.

The Neuron Chip RESET signals are connected together and wired to pin NCRES. A reset generator and low voltage detector is wired to NCRES as well. This low voltage detector monitors both the VCC and VCC3 rails. An open-collector driver can be used to pull NCRES low, to facilitate NCRREQ and FREQSEL mode changes after power on reset is complete. EEPROM refresh using NCRREQ is performed as discussed on the previous page.

The Neuron Chip SERVICE signals are connected to NCASVC and NCBSVC respectively. These can be monitored or connected to LEDs (8mA max.) if desired. Service switches and LEDs for NCASVC and NCBSVC are not required for network management and installation. The HEALTHY status signal will go inactive (high) if either NCASVC or NCBSVC go low during normal operation.

Table 2: Absolute Maximum Ratings

Description	Value	Units
VCC relative to GND	-0.3 to 6.0	V
VCC3 relative to GND	-0.5 to 4.0	V
Input voltage relative to GND (NCRREQ, FREQSEL)	-0.3 to (VCC + 0.3)	V
Input voltage relative to GND (NCRES, NCSVCA, NCSVCB)	-0.3 to min((VCC + 0.3), 5.5)	V
Input voltage relative to GND (PTRXD, PTRXCK, PTRXEN, PTRXPKT, BXID0, PKT, LTEST, THROTTLE, RCP1, RCP2, RESET, ASVC, BSVC, CLK20, CTS)	-0.5 to 5.5	V
Ambient storage temperature	-55 to 105	°C

Table 3: Reliability Characteristics

Parameter	Symbol	Min	Units
NCRREQ EEPROM Refresh Cycles	N_{ER}	10,000	Cycles
Neuron Chip EEPROM data retention (since last NCRREQ EEPROM refresh)	T_{NDR}	10	Years
CPLD program data retention	T_{CDR}	20	Years

Table 4: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage (5V)	V_{CC}	4.5	5.0	5.5	V
Supply voltage (3.3V)	V_{CC3}	3.0	3.3	3.6	V
High-level input voltage	V_{IH}	2.0		5.0	V
Low-level input voltage	V_{IL}	0		0.8	V
Ambient operating temperature	T_A	-40		85	°C

Table 5: DC Characteristics (over recommended operating conditions)

Parameter	Test Condition	Symbol	Min	Typ	Max	Units
Output low voltage	I_{OL} = 8mA	V_{OL}	0		0.4	V
Output high voltage (excluding open-collector outputs)	I_{OH} = -1.4mA	V_{OH}	2.4		VCC	V
Low-level input current (NCRREQ, FREQSEL, LTEST, ASVC, BSVC)	V_{IL} = 0V	$I_{IL(1)}$			1.6	mA
Low-level input current (NCRES, NCSVCA, NCSVCB)	V_{IL} = 0V	$I_{IL(2)}$			1.9	mA
Low-level input current (PTRXD, PTRXCK, PTRXEN, PTRXPKT, BXID0, PKT, THROTTLE, RCP1, RCP2, RESET, CLK20, CTS)	V_{IL} = 0V	$I_{IL(3)}$			0.30	mA
High-level input current (PTRXD, PTRXCK, PTRXEN, PTRXPKT, BXID0, PKT, THROTTLE, RCP1, RCP2, RESET, CLK20, CTS)	V_{IH} = 5V	$I_{IH(3)}$			-0.30	mA
Operating Current	V_{CC} = 5.0V, T_A = 25°C, 800 packets per second	I_{CC}		81		mA
Operating Current	V_{CC3} = 3.3V, T_A = 25°C, 800 packets per second	I_{CC3}		215		mA

Table 6: AC Characteristics (over recommended operating conditions)

Parameter	Symbol	Min	Typ	Max	Units
Transmit clock low time	t_{TCL}	195	200	205	ns
Transmit clock period	t_{TCP}	745	800	855	ns
Transmit packet and data setup time before rising PTTXCK	t_{TSU}	170			ns
Transmit packet and data hold time after rising PTTXCK	t_{TH}	520			ns
Receive clock low time	t_{RCL}	57			ns
Receive clock high time	t_{RCH}	57			ns
Receive clock period	t_{RCP}	122			ns
Receive packet and data setup time before rising PTRXCK	t_{RSU}	8			ns
Receive packet and data hold time after rising PTRXCK	t_{RH}	5			ns
Receive inter-packet gap	t_{RPH}	4			µs
THROTTLE frequency	f_{TH}	6		10,000	Hz
EEPROM refresh time (NCARACK, NCBRACK low time)	t_{ER}	4		41	S

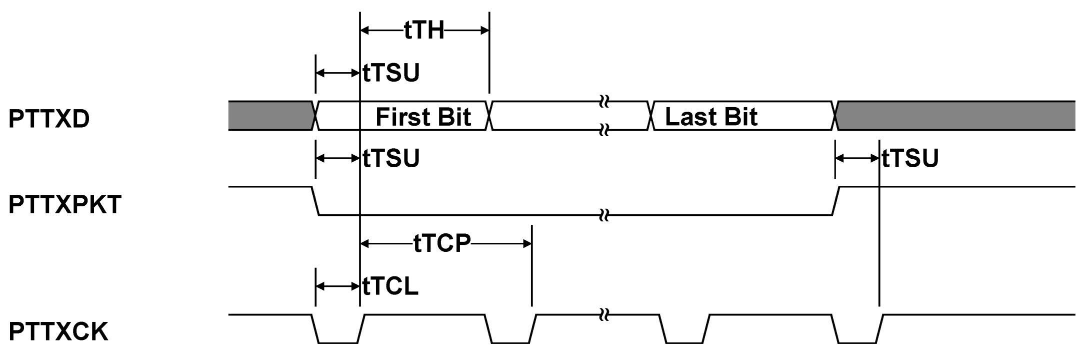


Figure 3: Foreign Protocol Interface Transmit Timing

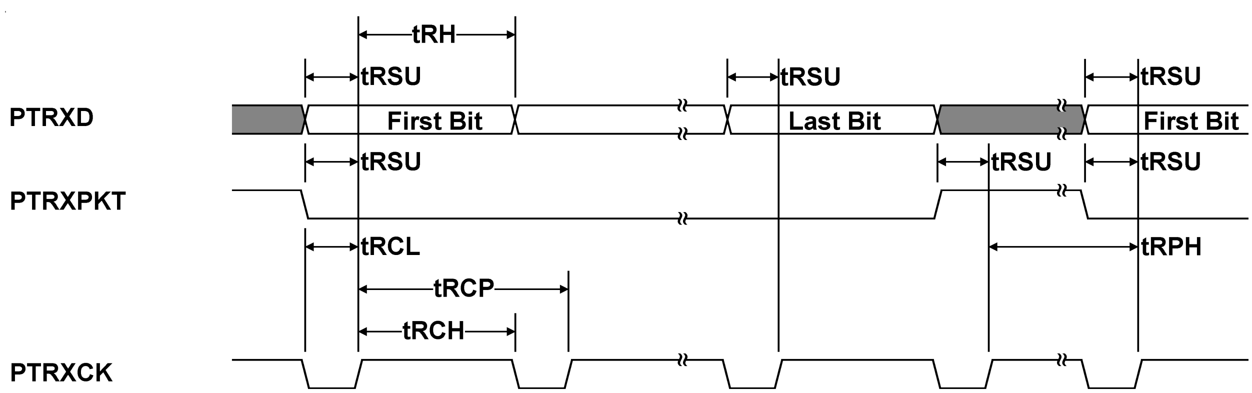


Figure 4: Foreign Protocol Interface Receive Timing

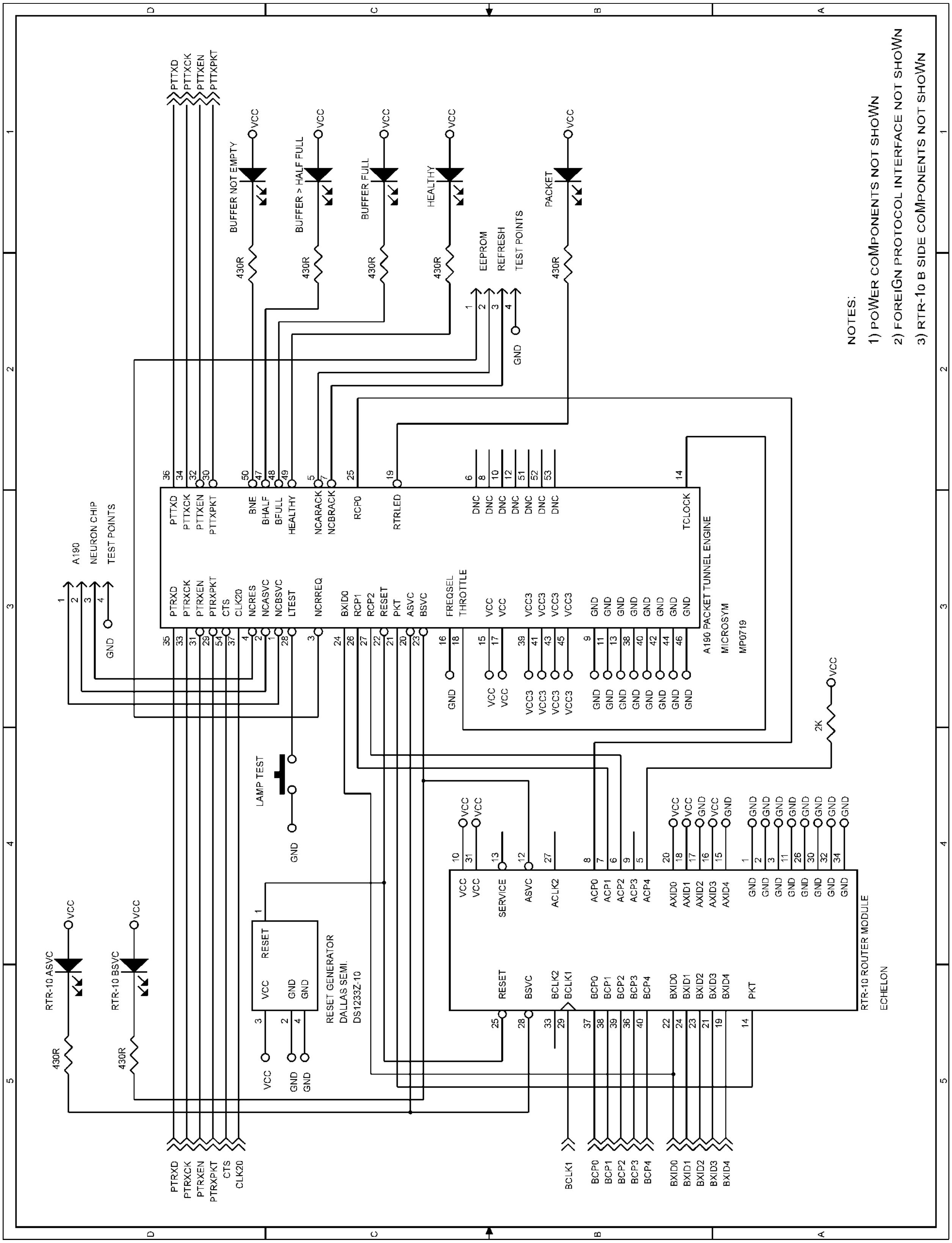


Figure 5: Example Application Schematic

Performance

The A190 bandwidth capability is equivalent to that of a standard TP/RS485-1250 channel.

Figure 6 shows test results for a pair of A190 tunneling routers connected back-to-back. For this test, both RTR-10s were connected to ten test nodes on TP/RS485-1250 channels. Each node both sent and received 12-byte (1 byte data plus 11 bytes overhead) messages to a corresponding node on the either side of the tunneling routers.

Lost packets can be due to collisions on the test node channels, or due to messages missed by the RTR-10s.

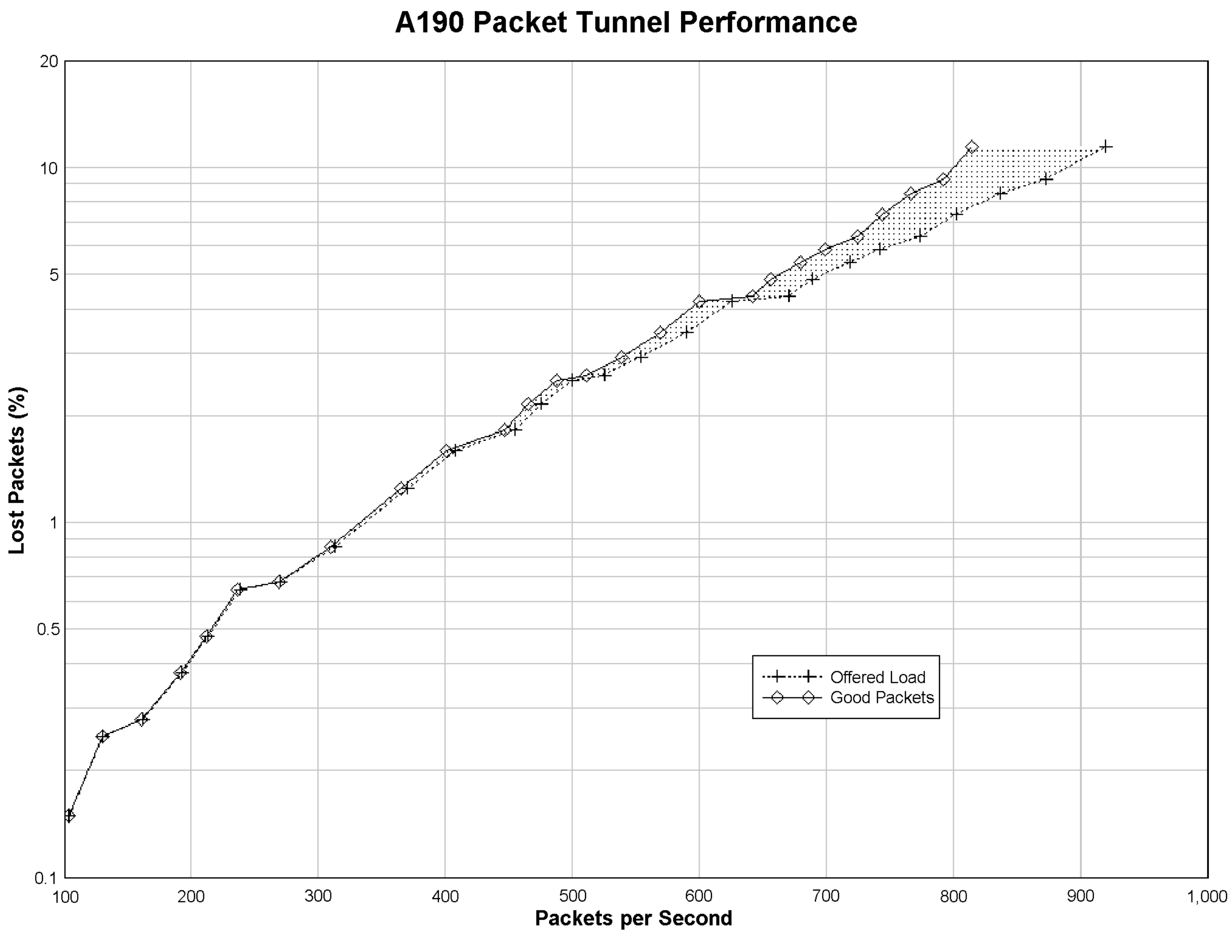


Figure 6: A190 Performance

Mounting

The A190 should be wave soldered to the target PCB. It can be mounted in sockets, but in this case there is no provision for mechanically securing the module. If sockets must be used, then Samtec SQT series sockets are compatible. Socket mounting is not recommended, except for test purposes.

Do not mount components on the target PCB under the A190 module.

Table 7 shows the mechanical coordinates of each pin, relative to the PCB footprint origin shown in figure 7. The pins are 0.020" (0.51mm) square. We recommend that the generated PCB footprint be checked against an actual A190, before a PCB is fabricated.

The pin material is phosphor bronze, 150µin tin plate over 50µin nickel.

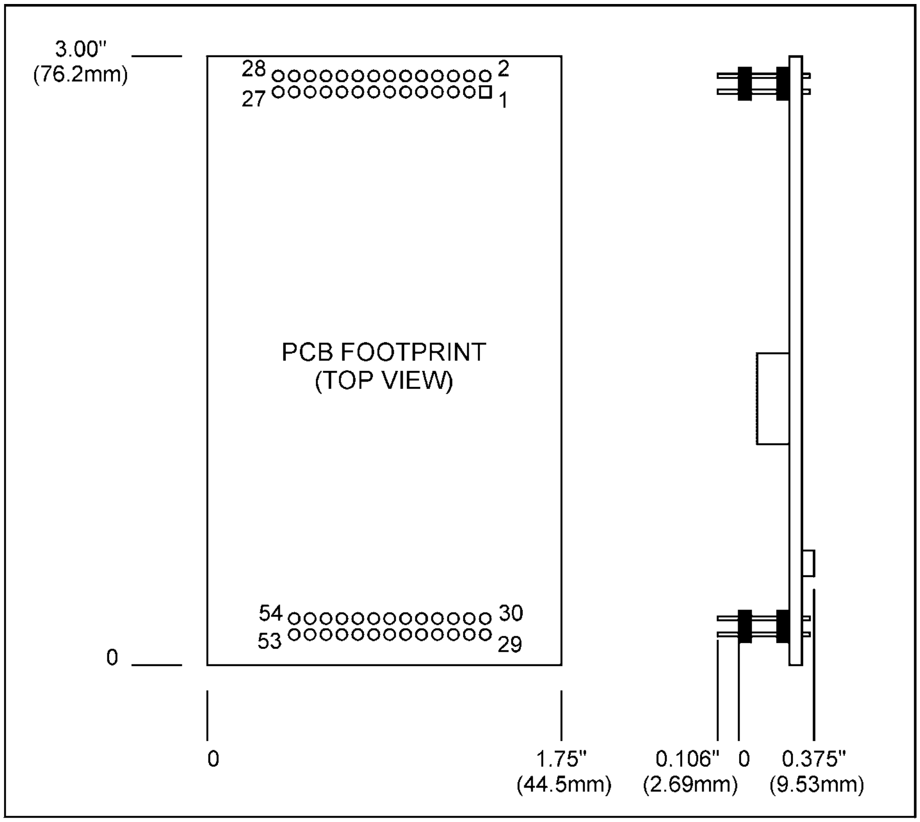


Figure 7: Mechanical Dimensions

Table 7: Pad Coordinates

Pin	Location (inches)		Location (millimeters)	
	X	Y	X	Y
1	1.375	2.825	34.93	71.76
2	1.375	2.904	34.93	73.76
3	1.296	2.825	32.93	71.76
4	1.296	2.904	32.93	73.76
5	1.218	2.825	30.93	71.76
6	1.218	2.904	30.93	73.76
7	1.139	2.825	28.93	71.76
8	1.139	2.904	28.93	73.76
9	1.060	2.825	26.93	71.76

Pin	Location (inches)		Location (millimeters)	
	X	Y	X	Y
10	1.060	2.904	26.93	73.76
11	0.981	2.825	24.93	71.76
12	0.981	2.904	24.93	73.76
13	0.903	2.825	22.93	71.76
14	0.903	2.904	22.93	73.76
15	0.824	2.825	20.93	71.76
16	0.824	2.904	20.93	73.76
17	0.745	2.825	18.93	71.76
18	0.745	2.904	18.93	73.76
19	0.666	2.825	16.93	71.76
20	0.666	2.904	16.93	73.76
21	0.588	2.825	14.93	71.76
22	0.588	2.904	14.93	73.76
23	0.509	2.825	12.93	71.76
24	0.509	2.904	12.93	73.76
25	0.430	2.825	10.93	71.76
26	0.430	2.904	10.93	73.76
27	0.351	2.825	8.93	71.76
28	0.351	2.904	8.93	73.76
29	1.375	0.150	34.93	3.81
30	1.375	0.229	34.93	5.81
31	1.296	0.150	32.93	3.81
32	1.296	0.229	32.93	5.81
33	1.218	0.150	30.93	3.81
34	1.218	0.229	30.93	5.81
35	1.139	0.150	28.93	3.81
36	1.139	0.229	28.93	5.81
37	1.060	0.150	26.93	3.81
38	1.060	0.229	26.93	5.81
39	0.981	0.150	24.93	3.81
40	0.981	0.229	24.93	5.81
41	0.903	0.150	22.93	3.81
42	0.903	0.229	22.93	5.81
43	0.824	0.150	20.93	3.81
44	0.824	0.229	20.93	5.81
45	0.745	0.150	18.93	3.81
46	0.745	0.229	18.93	5.81
47	0.666	0.150	16.93	3.81
48	0.666	0.229	16.93	5.81
49	0.588	0.150	14.93	3.81
50	0.588	0.229	14.93	5.81
51	0.509	0.150	12.93	3.81
52	0.509	0.229	12.93	5.81
53	0.430	0.150	10.93	3.81
54	0.430	0.229	10.93	5.81

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